AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Cancelled).

2. (Original) An analog-to-digital conversion circuit having a multi-stage pipeline structure composed of a plurality of stages of circuits for converting an analog input signal to a digital output value, wherein

each of the stages of circuits except the final stage includes:

an analog-to-digital converter that converts an inputted analog signal into a digital signal;

a digital-to-analog converter that converts the digital signal outputted from said analog-to-digital converter into an analog signal; and

a differential amplifier circuit that amplifies the difference between the inputted analog signal and the analog signal outputted from said digital-to-analog converter,

digital signals outputted from the analog-to-digital converters in said plurality of stages of circuits constituting said digital output value,

a correction value for correcting an error of said digital output value due to a gain error of said differential amplifier circuit in at least one stage of circuit of said plurality of stages being preset for each value of the digital signal outputted from said analog-to-digital converter in a subsequent stage of circuit,

said analog-to-digital conversion circuit comprising:

a correction value output circuit that outputs a corresponding correction value based on the digital signal outputted from said analog-to-digital converter in said subsequent stage of circuit; and

a correction circuit that corrects said digital output value based on the correction value outputted from said correction value output circuit.

3. (Original) The analog-to-digital conversion circuit according to claim 2, wherein

said correction value output circuit includes:

a storage circuit that stores a correction value for each value of the digital signal outputted from said analog-to-digital converters in said subsequent stage of circuit; and

a selection circuit that selects a corresponding correction value among said correction values stored in said storage circuit based on the digital signal outputted from said analog-to-digital converter in said subsequent stage of circuit for output.

4. (Original) The analog-to-digital conversion circuit according to claim 3, wherein

said storage circuit stores a plurality of groups of correction values each group of correction values being set for each value of the digital signal outputted from said analog-to-digital converter in said subsequent stage of circuit, and

said selection circuit selects a corresponding correction value among said correction values stored in said storage circuit based on a predetermined control signal and the digital signal outputted from said analog-to-digital converter in said subsequent stage of circuit for output.

5. (Original) The analog-to-digital conversion circuit according to claim 4, further comprising:

an error detector that detects an error of said digital output value due to the gain error of said differential amplifier circuit in said one stage of circuit; and

a control signal generator that generates said control signal based on the error detected by said error detector.

6. (Original) The analog-to-digital conversion circuit according to claim 4, further comprising:

a control signal holder that holds said control signal preset based on an error of said digital output value due to the gain error of said differential amplifier circuit in said one stage of circuit.

7. (Original) The analog-to-digital conversion circuit according to claim 2, wherein said one stage of circuit is an initial stage of circuit.

8. (Original) An analog-to-digital conversion circuit having a multi-stage pipeline structure composed of a plurality of stages for converting an analog signal into a digital output value, wherein

at least one stage of circuit of said plurality of stages of circuits comprises:

a comparator that compares an inputted analog signal with a reference voltage;

an operational amplifier that operates in response to an output signal from said comparator; and

a first switch that selectively inputs a reference voltage equivalent to said reference voltage and said analog signal,

said analog-to-digital conversion circuit correcting an interstage gain error using the digital output value obtained when said equivalent reference voltage is inputted.

9. (Original) An analog-to-digital conversion circuit having a multi-stage pipeline structure composed of a plurality of stages for converting an analog signal into a digital output value, wherein

at least one stage of circuit of said plurality of stages of circuits comprises:

a comparator that compares an inputted analog signal with a reference voltage;

an operational amplifier that operates in response to an output signal from said comparator;

a first switch that selectively inputs a reference voltage equivalent to said reference voltage and said analog signal; and

a signal generation circuit that generates a first signal having a first logic value and a second signal having a second logic value,

said operational amplifier operating in response to the first signal and second signal generated by said signal generation circuit when said equivalent reference voltage is inputted to said comparator by said first switch.

10. (Original) An analog-to-digital conversion circuit having a multi-stage pipeline structure composed of a plurality of stages for converting an analog signal into a digital output value, wherein

each of the stages of circuits except the final stage comprises:

an analog-to-digital converter that converts an inputted analog signal into a digital signal;

a digital-to-analog converter that converts the digital signal outputted from said analog-to-digital converter into an analog signal; and

a differential amplifier that amplifies the difference between the inputted analog signal and the analog signal outputted from said digital-to-analog converter,

said analog-to-digital converter including:

a plurality of comparators that compare said inputted analog signal with a plurality of reference voltages respectively; and

an encoder that encodes output signals from said plurality of comparators to generate a digital signal,

at least one stage of circuit of said plurality of stages of circuits including:

a first switch that selectively inputs an analog signal supplied from an external source or preceding stage of circuit and a reference voltage equivalent to the reference voltage supplied to at least one comparator of said plurality of comparators;

a signal generation circuit that generates a first signal having a first logic value and a second signal having a second logic value; and

a second switch that supplies output signals from said digital-to-analog converter corresponding to the first signal and second signal generated by said signal generation circuit to said differential amplifier when said equivalent reference voltage is inputted by said first switch.

11. (Original) The analog-to-digital conversion circuit according to claim 10, wherein

the voltage range in the stage of circuit subsequent to said at least one stage of circuit includes a normal range and a redundant range, and

said equivalent reference voltage is an arbitrary voltage within an area where said normal range including a reference voltage supplied to said at least one comparator and said redundant range overlap with each other.

12. (Original) The analog-to-digital conversion circuit according to claim 10, further comprising a subtracter that calculates the difference between the digital output value obtained when said first signal is supplied to said encoder and the digital output value obtained when said second signal is supplied to said encoder.

13. (Original) The analog-to-digital conversion circuit according to claim 12, further comprising a correction circuit that corrects the digital output value based on an output signal from said subtracter.

14. (Original) The analog-to-digital conversion circuit according to claim 10, wherein

said first switch selectively inputs an analog signal supplied from an external source or preceding stage of circuit and a plurality of reference voltages equivalent to the plurality of reference voltages supplied respectively to a plurality of comparators among said plurality of comparators, and

said second switch supplies the first signal and second signal generated by said signal generation circuit to said encoder in place of the output signal from the corresponding

comparator when any of said plurality of equivalent reference voltages is inputted by said first switch.

15. (Original) The analog-to-digital conversion circuit according to claim 10, wherein

said at least one stage of circuit includes a plurality of stages of circuits, and

each of said plurality of stages of circuits includes:

a first switch that selectively inputs an analog signal supplied from an external source or preceding stage of circuit and a reference voltage equivalent to the reference voltage supplied to at least one comparator of said plurality of comparators;

a signal generation circuit that generates a first signal having a first logic value and a second signal having a second logic value; and

a second switch that sequentially supplies the first signal and second signal generated by said signal generation circuit to said encoder in place of the output signal from said at least one comparator, when said equivalent reference voltage is inputted by said first switch.

16. (Original) An analog-to-digital conversion circuit comprising:

a first circuit having a first and second nodes;

a selector that selectively supplies one of an inputted analog signal and an analog signal at said second node to said first node; and

a control device that controls said first switch, wherein

said first circuit includes:

an analog-to-digital converter that converts the analog signal from said first node into a digital signal;

a digital-to-analog converter that converts the digital signal outputted from said analog-to-digital converter into an analog signal; and

a differential amplifier that amplifies the difference between the analog signal from said first node and the analog signal outputted from said digital–to-analog converter and outputs the amplified difference to said second node,

said control device controls said selector such that conversion operation of said analog-to-digital converter, conversion operation of said digital-to-analog converter, and amplifying operation of said differential amplifier are carried out a predetermined number of cycles after the inputted analog signal is supplied to said first node,

said analog-to-digital converter includes:

a plurality of comparators that compare said inputted analog signal with a plurality of reference voltages respectively; and

an encoder that encodes output signals from said plurality of comparators to generate a digital signal,

said first circuit includes:

a first switch that selectively inputs an analog signal supplied from an external source or preceding stage of circuit and a reference voltage equivalent to the reference voltage supplied to at least one comparator of said plurality of comparators;

a signal generation circuit that generates a first signal having a first logic value and a second signal having a second logic value; and

a second switch that supplies the output signals from said digital-to-analog converter corresponding to the first signal and second signal generated by said signal generation circuit to said differential amplifier when said equivalent reference voltage is inputted by said first switch.

17. (Original) The analog-to-digital conversion circuit according to claim 16, wherein the voltage range in said first circuit includes

a normal range and a redundant range, and

said equivalent reference voltage is an arbitrary voltage within an area where said normal range including the reference voltage supplied to said at least one comparator and said redundant range overlap with each other.

18. (Original) The analog-to-digital conversion circuit according to claim 16, further comprising a subtracter that calculates the difference between the digital output value obtained when said first signal is supplied to said encoder and the digital output value obtained when said second signal is supplied to said encoder.

19. (Original) The analog-to-digital conversion circuit according to claim 18, further comprising a correction circuit that corrects the digital output value based on an output signal from said subtracter.

20. (Original) An analog-to-digital conversion circuit having a multi-pipeline structure composed of a plurality of stages of circuits for converting an analog signal to a digital output value, wherein

at least one stage of circuit of said plurality of stages of circuits includes:

an analog-to-digital converter that converts an inputted analog signal into a digital signal;

a digital-to-analog converter that converts the digital signal outputted from said analog-to-digital converter into an analog signal;

an operational amplifier that amplifies the inputted analog signal;

a differential amplifier that amplifies the difference between the analog signal outputted from said operational amplifier and the analog signal outputted from said digital-to-analog converter;

a comparator that compares said inputted analog signal with a reference voltage;

an adjustment circuit that adjusts a voltage range of the analog signal inputted to said operational amplifier and a voltage range in said digital-to-analog converter based on the output signal from said comparator;

a first switch that selectively inputs an inputted analog signal and a reference voltage equivalent to the reference voltage supplied to said comparator;

a signal generation circuit that generates a first signal having a first logic value and a second signal having a second logic value; and

a second switch that sequentially supplies the first signal and second signal generated by said signal generation circuit in place of the output signal from said comparator when said equivalent voltage is inputted by said first switch.

Claim 21 (Cancelled).